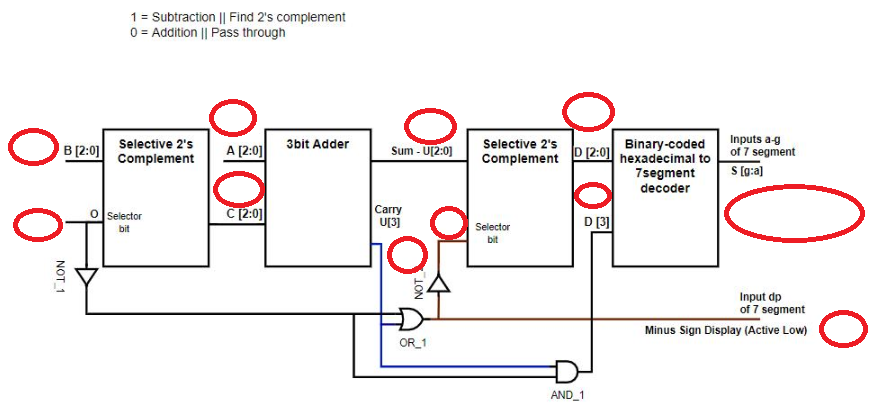
# Lab 06 – Worksheet

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## Introduction

Label the figure below *or* type test cases which you have performed on given design during the lab:



| B[2:0] = 010  O = 1  A[2:0] = 110  C [2:0] = 110 (2’s complement of 010)  U [3:0] = 1100  **U[2:0] = 100** **-> Answer**  U[3] = 1  Selector Bit for 2nd “Selective 2’s Complement” = 0  D[2:0] = 100 (U[2:0] will not be complemented as Selector Bit is 0)  D[3] = 0 {AND of 0 [NOT of O(1) = 0] and [Carry U(3) = 1]}  **dp = 1** (1 means off for active Low so it’s positive)  . Verifying:  110 - 010 = 100 (binary), correct.  5 - 2 = 3 (decimal), corrent. |
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1. **7-Segment Hexadecimal Display Decoder**

Table 6.1

| **Hex Digit** | **Binary-coded Hexadecimal/ Inputs to decoder** | | | | **Outputs of the decoder** | | | | | | |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **D3** | **D2** | **D1** | **D0** | **Sg** | **Sf** | **Se** | **Sd** | **Sc** | **Sb** | **Sa** |
| 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 2 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 3 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 4 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| 5 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| 6 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| 7 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 8 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 9 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| A | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| B | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| C | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| D | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| E | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| F | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 |

Write Boolean expression for each output segment.

Table 6.2

| Sa = | D3’D2’D1’D0 + D3’D2D1’D0+D3D2’D1D0+D3D2D1’D0 |
| --- | --- |
| Sb = | D2D1D0 + D3D1D0 + D3D2D0’+D3’D2D1’D0 |
| Sc = | D3D2D0’ + D3D2D1 + D3’D2’D1D0’ |
| Sd = | D2D1D0 + D3’D2’D1’D0  + D3’D2D1’D0’ + D3D2’D1D0’ |
| Se = | D3’D0+D2’D1’D0+D3’D2D1’ |
| Sf = | D3’D2’D0 + D3’D2’ D1 + D3’D2D1’D0 |
| Sg = | D3’D2’D1’ + D3’D2D1D0 + D3D2D1 D0’ |

*Appropriately add comments to your code and* ***write*** *the code of your design module in the box below.*

| `timescale 1ns / 1ps  module SevenSegment(  input [3:0] D,  output [6:0] S);    assign S[0] = (~D[3]&~D[2]&~D[1]&D[0] | ~D[3]&D[2]&~D[1]&~D[0] | D[3]&~D[2]&D[1]&D[0] | D[3]&D[2]&~D[1]&D[0]);  assign S[1] = (D[2]&D[1]&~D[0] | D[3]&D[1]&D[0] | D[3]&D[2]&~D[0] | ~D[3]&D[2]&~D[1]&D[0]);  assign S[2] = (D[3]&D[2]&~D[0] | D[3]&D[2]&D[1] | ~D[3]&~D[2]&D[1]&~D[0]);  assign S[3] = (D[2]&D[1]&D[0] | ~D[3]&~D[2]&~D[1]&D[0] | ~D[3]&D[2]&~D[1]&~D[0] | D[3]&~D[2]&D[1]&~D[0]);  assign S[4] = (~D[3]&D[0] | ~D[2]&~D[1]&D[0] | ~D[3]&D[2]&~D[1]);  assign S[5] = (~D[3]&~D[2]&D[0] | ~D[3]&~D[2]&D[1] | ~D[3]&D[1]&D[0] | D[3]&D[2]&~D[1]&D[0]);  assign S[6] = (~D[3]&~D[2]&~D[1] | ~D[3]&D[2]&D[1]&D[0] | D[3]&D[2]&~D[1]&~D[0]);    endmodule |
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*Attach RTL Schematic of the module.*

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*Attach screenshot of your simulation output window*: (Invert background color to white using settings option in simulation window)

|  |
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## Adder/Subtractor system

*Provide code for design module here*

| `timescale 1ns / 1ps  module Adder(  input a,  input b,  input c,  output sum,  output carry  );    wire x1,x2,x3;  xor(x1,a,b);  xor g2(sum,c,x1);  and(x2,c,x1);  and(x3,a,b);  or(carry,x2,x3);  endmodule  module ThreeBitFullAdder(  input [2:0] A,  input [2:0] B,  output [2:0] Y,  output Cout  ); |
| --- |

*Add your testbench here*

| *`timescale 1ns / 1ps*  *module ThreeBitAdderSimulation();*  *reg [2:0] A;*  *reg [2:0] B;*  *wire [2:0] Y;*  *wire Cout;*  *ThreeBitFullAdder module\_u\_test (A, B , Y, Cout);*  *initial begin*  *#100 A = 3'b111;*  *B = 3'b001;*  *#100 A = 3'b000;*  *B = 3'b101;*  *#100 A = 3'b001;*  *B = 3'b110;*  *#100 A = 3'b011;*  *B = 3'b010;*  *end*  *endmodule* |
| --- |

*Attach screenshot of waveform results here* (Invert background color to white using settings option in simulation window)

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## Assessment Rubrics

**Marks Distribution:**

|  |  | **LR2**  **Code** | **LR4**  **Data**  **Collection** | **LR5**  **Results** | **LR7**  **Viva** | **LR9**  **Report** |
| --- | --- | --- | --- | --- | --- | --- |
| **In-lab** | **Task a** |  |  |  | 10 points | 10 points |
| **Task b** | 15 points | 20 points | 15 points |  |
| **Task c** | 20 points |  | 10 points |  |
| **Total Marks =** |  | 100 points | | | | |

**Marks Obtained:**

|  |  | **LR2**  **Code** | **LR4**  **Data**  **Collection** | **LR5**  **Results** | **LR7**  **Viva** | **LR9**  **Report** |
| --- | --- | --- | --- | --- | --- | --- |
| **In-lab** | **Task a** | - | - | - |  |  |
| **Task b** |  |  |  | - |
| **Task c** |  | - |  | - |
| **Total Marks =** |  |  | | | | |